IN THE CLAIMS

No claims are amended, added, or cancelled in this response.

INTRODUCTORY COMMENTS

Reconsideration of this application is respectfully requested. Claims 31-57 are currently pending and stand rejected in the application.

Rejections Under 35 U.S.C. § 102(e)

In the office action dated May 19, 2004, claims 31-44, 45, and 47-55 stand rejected under 35 U.S.C. §102(e) as anticipated by US 6,555,208 of Takada, et al. (hereafter Takada). The office action asserts "Takada discloses, referring to figure 4, a printed circuit board (PCB) comprising:...at least one padless via (203) extending from the first signal routing layer to the electrically conductive layer, the at least one padless via in electrical contact with the electrically conductive layer (see col. 14, lines 10-20)." (Office action, page 2, paragraph 4.) The office action further states applicants' arguments that Takada fails to teach a padless via are not persuasive. The office action asserts that Takada's stated "*the above conductor pattern* is all conductive patterns which are able to be formed on the surface of the insulating substrate such as a wiring circuit . . ." teaches a padless via on the grounds that a wiring circuit is "fundamentally different from [a] pad", (Office action, page 8, paragraph 1) (emphasis provided). Applicants respectfully submit the office action misconstrues the Takada recitation, and when properly read in context, Takada's recitation supports applicants arguments.

The recitation cited by the office action is found in Takada's description of "[a] third invention", (column 6, line 66 – column 7, line 2). The office action asserts that 'the above conductor pattern' teaches a pattern on the surface of substrate that is a part of Takada's invention. However, Takada explicitly discloses "*a pad* for external connection arranged in an outermost layer of the insulating substrate, a *conductor pattern* arranged in another layer *different from said outermost layer*, and a hole for conductivity for electrically connecting said pad for external connection and said conductor pattern", (column 6, lines 21-26) (emphasis provided). Here Takada discloses the required presence of a pad on the outer layer in accordance with applicant's prior arguments. Takada also discloses that the conductor pattern cited by the office action is 'in another layer different from said outermost layer', the aforementioned outermost layer being the one containing the pad described by Takada. Lastly, Takada discloses that the pad and the conductor pattern are different features of the same invention, and therefore, the conductor pattern, "such as a wiring circuit..." does not obviate the requirement for a pad in Takada's invention, but co-exists with it as disclosed. Takada discloses, "[t]he pad for external connection is arranged so as to form the bottom portion of the hole for conductivity. Therefore, it is not necessary to form a conductor pattern for connecting the hole for conductivity and the pad for external connection", (column 6, lines 35-39). Here, Takada discloses that the pad 'is arranged so as to form the bottom portion of the hole', wherein the hole and the pad are integrated, thus disclosing a via with a pad, not a 'padless' via as claimed by applicants.

Therefore, although Takada discloses that the 'conductor pattern' recited in the office action may comprise a wiring circuit, applicants have shown that Takada

also expressly requires a pad at "at least one area of the opening portion of the hole", forming a via which is not 'padless'. Likewise, as previously demonstrated by applicants in the response filed 24 January 2005, vias with pads, and not padless vias, are disclosed throughout Takada. Therefore, applicants respectfully submit that Takada fails to teach applicants' recitation of "at least one padless via".

For at least the reason that Takada fails to teach applicants' recitation of "at least one padless via", recited in applicants independent claims 31, 36, 41, 47, and 54, applicants respectfully submit that the 35 U.S.C. §102(e) rejection of each of these claims is improper, and request the rejections be withdrawn. In as much as claims 32-35, 37-40, 42-44, 48-53, and 55 depend from and include the recitations of independent claims 31, 36, 41, 47, and 54, respectively, applicants submit the 35 U.S.C. §102(e) rejection of each of these claims is likewise improper and request the rejections be withdrawn.

Rejections Under 35 U.S.C. § 103(a)

In the office action, claim 44 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Takada. The office action asserts that Takada discloses the claimed invention, except that Takada does not specifically state that a width of the at least two conductive traces is approximately 3 mils. Instead, Takada generically states that the width can be varied, (Takada, column 15, lines 25-35). Thus, the office action asserts that forming the claimed traces with a width of 3 mils would be obvious to one of ordinary skill in the art at the time of the invention, (office action, page 6, paragraph 2). Applicants respectfully disagree that this is so.

As applicants demonstrated in the prior section, Takada fails to disclose applicants' invention, including the recitation cited in the office action, in as much as Takada fails to disclose the at least one padless via.

Therefore, applicants respectfully submit that the U.S.C. §103(a) rejection of claim 44 is improper and should be withdrawn, as Takada fails to disclose or make obvious the applicants' claimed invention including the at least one padless via.

The office action further rejects claims 46, 56, and 57 under 35 U.S.C. 103(a) as being unpatentable over Takada in light of US 2003/0001287 (hereafter Sathe), (office action, page 6, paragraph 4). The office action asserts that Takada discloses the claimed invention, except Takada does not specifically state that the PCB is a motherboard and the component is a processor. However, the office action further asserts that the disclosure of Sathe demonstrates it is well known in the art that Takada's PCB could be considered a motherboard, and that processors are attached to said boards, (office action, page 7, paragraph 1) Additionally, the office action states that at the time of invention, it would have been obvious to comprise the component of a well known BGA package or LGA package, (office action, page 7, paragraph 2) Therefore, the office action asserts it would have been obvious to one having ordinary skill in the art, at the time of invention, to comprise the board and component in Takada of a motherboard and processor respectively.

As applicants demonstrated in discussion of the 35 U.S.C. 102(e) rejection, Takada fails to disclose applicants' invention in as much as Takada fails to disclose the at least one padless via claimed in independent claims 41 and 54, from which claims 46, and 56 & 57 depend, respectively. As cited in the office action, the recitations of Sathe

are unrelated to padless vias, and so the combination of Takada with Sathe also fails to teach or make obvious applicants' invention including the at least one padless via.

Therefore, applicants respectfully submit that the U.S.C. §103(a) rejection of claim 46, 56 & 57 is improper and should be withdrawn. Takada fails to disclose the at least one padless via in applicants' independent claims, and the cited combination of Takada with Sathe fail to make obvious applicants' invention including the at least one padless via. Therefore, the combined references are improper as a basis for a 35 U.S.C. 103(a) rejection for claims 46, 56, and 57.

CONCLUSION

In light of the points and arguments set forth herein, applicants respectfully submit that the rejections have been properly overcome, and the claims are allowable as they stand.

Please charge any shortages and credit any overages to Deposit Account No. 02-2666.

Respectfully submitted,

Date: June 10, 2005

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On: June 10, 2005
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Rachael Brown
Date 6/10/05